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Design Of Efficient BCD Adders In Quantum Dot Cellular Automata

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Abstract: *Among the emerging technologies recently proposed as alternatives to the classic CMOS, Quantum-dot cellular automata (QCA) is one of the most promising solutions to design ultra low-power and very high speed digital circuits. Efficient QCA-based implementations have been demonstrated for several binary and decimal arithmetic circuits, but significant improvements are still possible if the logic gates inherently available within the QCA technology are smartly exploited. This brief proposes a new approach to design QCA-based BCD adders. Exploiting innovative logic formulations and purpose designed QCA modules, computational speed significantly higher than existing counterparts are achieved without sacrificing either the occupied area or the cells count.*
Keywords: *QCA, CMOS, BCD*

I. Introduction

Quantum-dot cellular automata(QCA) has been recognized as one of the technologies that may replace field-effect transistor (FET)-based computing devices at the nano-scale level. Current complementary metal oxide semiconductor technology is going to approach a scaling limit in deep nanometer technologies. The current silicon transistor technology faces challenging problems, such as high-power consumption and difficulties in feature size reduction. Nanotechnology is an alternative to these problems, and the international technology roadmap for semiconductors (ITRS) report summarizes several possible technology solutions. Quantum-dot cellular automata(QCA) is a nanotechnology that offers a new method of computation and information transformation.

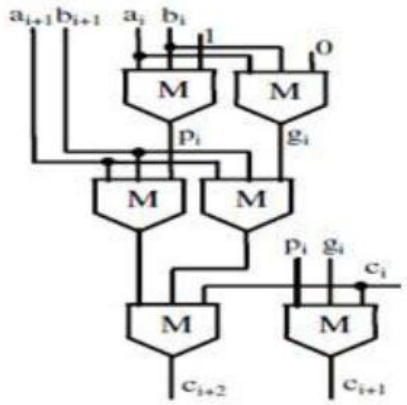


Fig 1: Novel 2-bit QCA module.

II. Existing System

The main objective of this paper is to perform both BCD addition and BCD subtraction in a single circuit with minimum number of garbage gate count and constant input. To achieve the operation of reversible BCD addition and subtraction in a single circuit two new gates are proposed which are optimized such that it doesn't possess any restrictions of reversible gates as mentioned above. It has been proved that the proposed reversible BCD arithmetic circuit is better than the existing logics in the literature; in terms of number of garbage outputs, constants inputs and the gate count

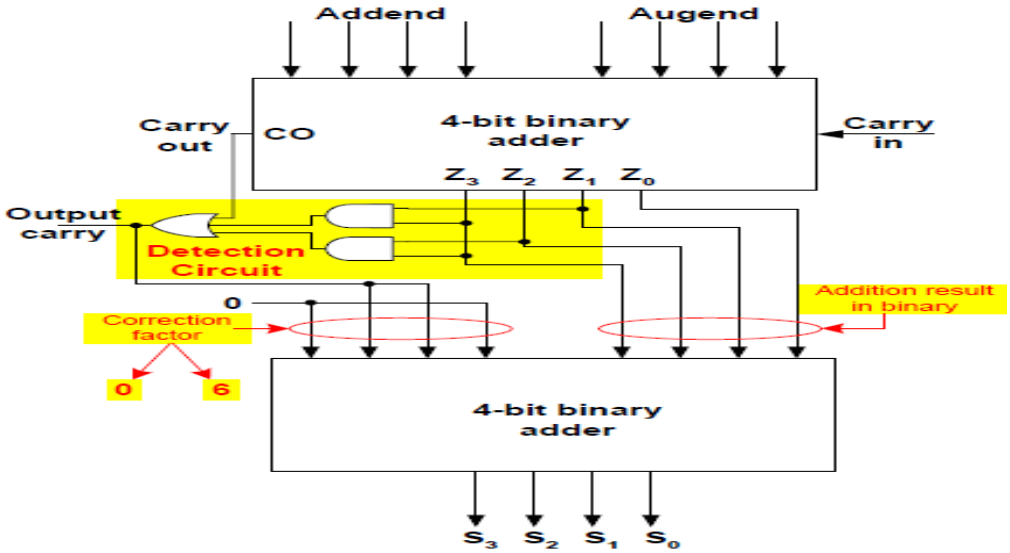


Fig 2: The conventional block diagram of BCD.

BCD or Binary Coded Decimal is that number system or code which has the binary numbers or digits to represent a decimal number. A decimal number contains 10 digits (0-9). Now the equivalent binary numbers can be found out of these 10 decimal numbers. In case of BCD the binary number formed by four binary digits, will be the equivalent code for the given decimal digits. In BCD we can use the binary number from 0000-1001 only, which are the decimal equivalent from 0-9 respectively. Suppose if a number have single decimal digit then it's equivalent Binary Coded Decimal will be the respective four binary digits of that decimal number and if the number contains two decimal digits then it's equivalent BCD will be the respective eight binary of the given decimal number. Four for the first decimal digit and next four for the second decimal digit. It may be cleared from an example.

QCA BCD Adder

A Binary Coded Decimal (BCD) adder is a circuit which adds two 4-bit BCD numbers in parallel and produces a 4-bit BCD result. Fig. 1 shows the block diagram of conventional BCD adder. The circuit must include the correction logic to produce valid BCD output. Two 4-bit BCD numbers X and Y along with carry input is added using conventional 4-bit parallel adder, 4-bit sum and a carry is taken out. If the carry output is set or if the result is greater than nine, binary 0110 is added to the intermediate sum output with the help of second stage 4-bit parallel adder circuit.

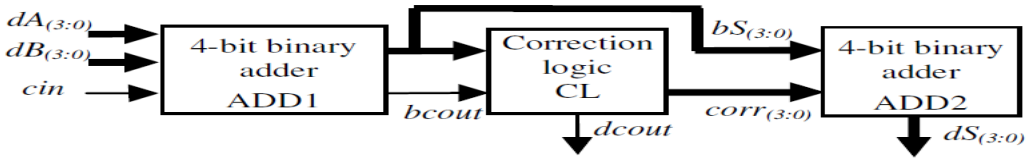


Fig 3: BCD adders using QCA.

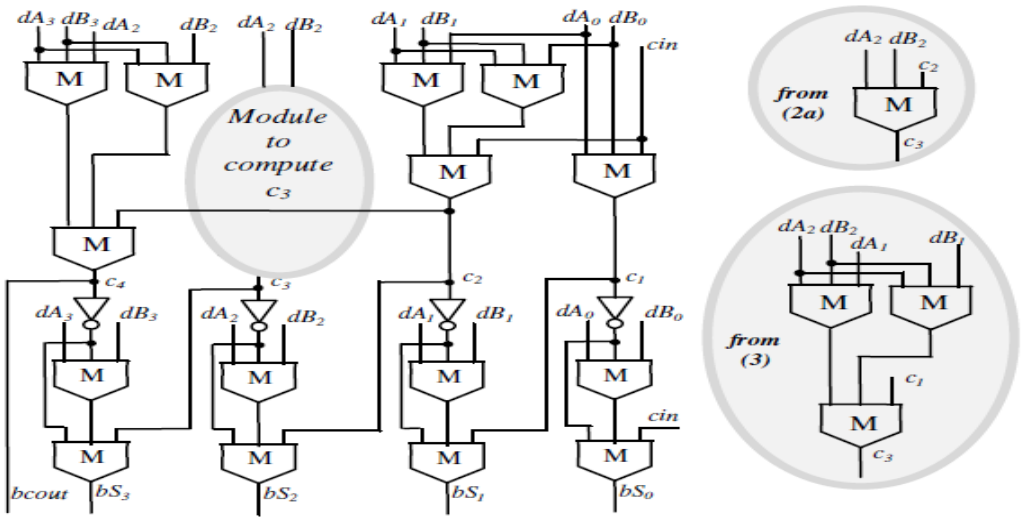


Fig. 4 The new ADD1 module.

Disadvantages:
The existing QCA BCD adder is only one-digit, limited bit resource bit operation, we can't implement n-digit BCD Adder

III. Proposed System

A novel QCA adder design is presented that reduces the number of QCA cells when compared to previously reported designs. We demonstrate that it is possible to design a CLA QCA one-bit adder, with the same reduced hardware as the bit-serial adder, while retaining the simpler clocking scheme and parallel structure of the original CLA approach. The proposed structure is based on a new algorithm that requires only three majority gates and two inverters for the QCA addition. It is noted that the bit-serial QCA adder uses a variant of the proposed one-bit QCA adder. By connecting n proposed one-bit QCA adders, we can obtain an efficient n-bit QCA adder with CLA.

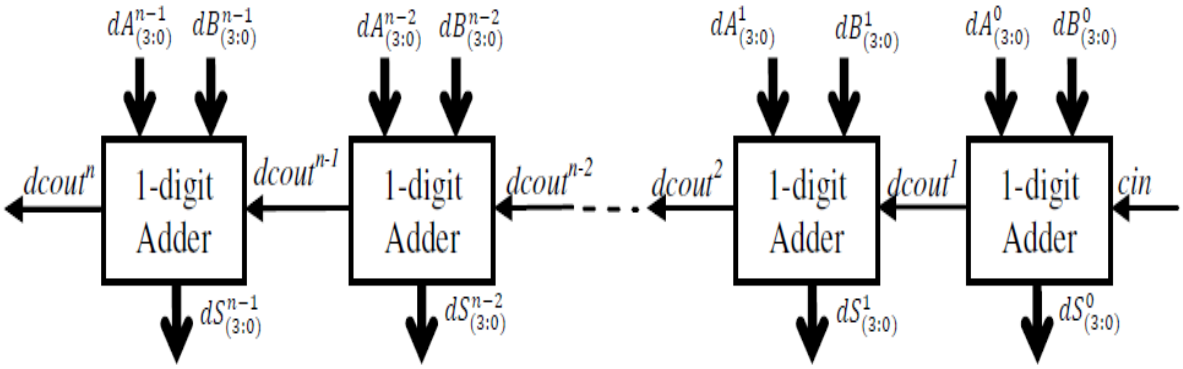


Fig: 5 The Proposed n-digit BCD adder.

The BCD adder here presented follows the traditional top-level structure illustrated in Fig.5,. As the main result, the proposed approach leads to the best trade-off between the overall occupied area and the speed performances.

To understand the new design strategy, let's examine first the 4-bit binary adder ADD1. It receives the digits dA(3:0) and dB(3:0) and the carry cin as inputs, and computes the binary results bcout and bS (3:0). Demonstrates that, for QCA-based rippling adders, the optimal logic structure for propagating a carry Ci through a single bit position is represented by that introduces only one MG between Ci and Ci+1.

ADVANTAGE
The proposed BCD adder is a implement n-digit BCD Adder using QCA can achieve high device density, extremely low power consumption, and very high switching speed

IV. Simulation& Synthesis Results

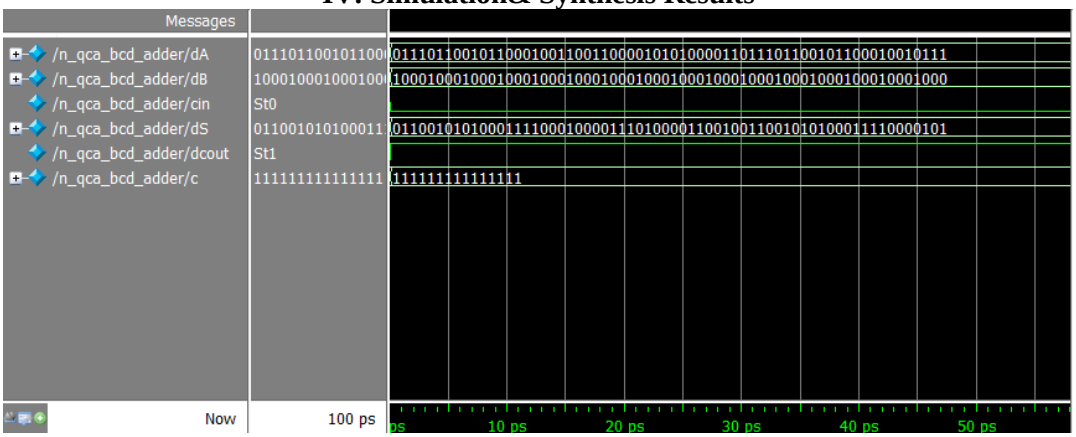


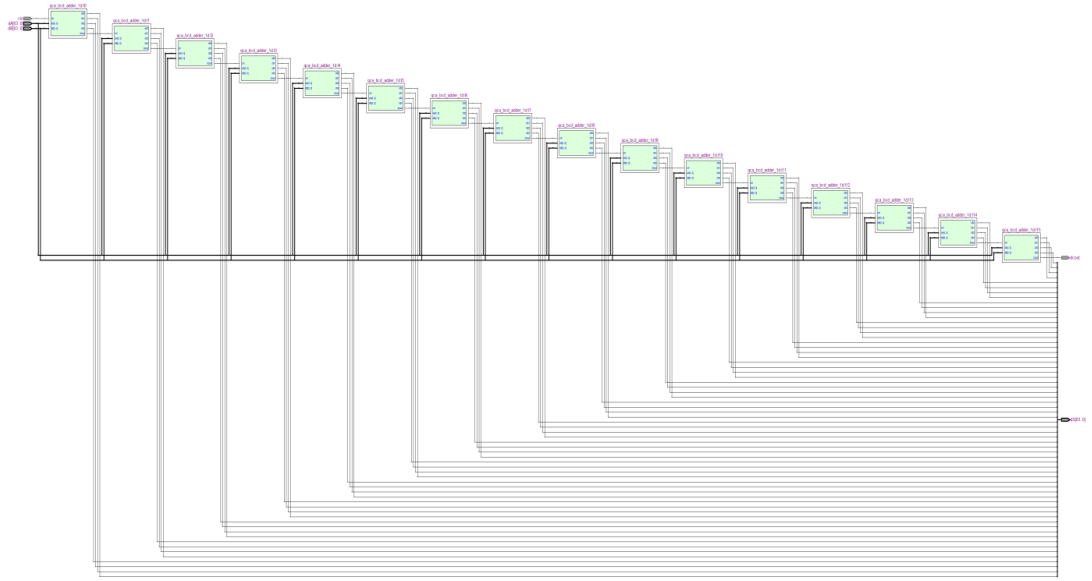
Fig.6 16 digit BCD adder

Area Optimization result

Flow Summary

Flow Status	Successful - Sat Oct 08 16:10:40 2016
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	n_qca_bcd_adder
Top-level Entity Name	n_qca_bcd_adder
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	195 / 33,216 (< 1 %)
Total combinational functions	195 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	194 / 475 (41 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

RTL VIEW



V. Conclusion

A new design approach has been presented and demonstrated to achieve efficient QCA-based implementations of decimal adders. Unconventional logic formulations and purpose-designed logic modules here proposed allows outperforming decimal adders known in literature. In fact, the new 1-digit BCD adder exhibits computational delay and area occupancy and lower than existing competitors. These advantages become even more evident when two n-digit decimal numbers must be summed.

References

[1]. C.S.Lent, P.D.Tougaw, W.Porod, G.H.Bernestein, "Quantum Cellular Automata", Nanotechnology, Vol.4, n°1, pp.49-57, 1993.
[2]. V.Pudi, K.Sridharan, "New decomposition theorems on majority logic for low-delay adder design in quantum dot cellular automata", IEEE Transactions on Circuits and Systems II: Express Brief, Vol.59, n°10, pp.678-682, 2012.
[3]. H.Cho, E.E.Swartzlander Jr., "Adder Design and Analyses for Quantum-Dot Cellular Automata", IEEE Transactions on Nanotechnology, Vol.6, n°3, pp.374-383, 2007.
[4]. H.Cho, E.E.Swartzlander Jr., "Adder and Multiplier Design in Quantum-Dot Cellular Automata", IEEE Transactions on Computers, Vol.58, n°6, pp.721-727, 2009.
[5]. V.Pudi, K.Sridharan, "Efficient Design of a Hybrid Adder in Quantum- Dot Cellular Automata", IEEE Transactions on VLSI Systems, Vol.19, n°9, pp.1535-1548, 2011.
[6]. S.Perri, P.Corsonello, G.Cocorullo, "Area-Delay Efficient Binary Adders in QCA", IEEE Transactions on VLSI Systems, Vol.22, n°5, pp.1174-1179, 2014.
[7]. L.Lu, W.Liu, M.O'Neill, E.E.Swartzlander Jr., "QCA Systolic Array Design", IEEE Transactions on Computers, Vol.62, n°3, pp.548-560, 2013.